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**UTILITY PATENT APPLICATION TRANSMITTAL**  
(Only for new nonprovisional applications under 37 CFR 1.53(b))

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ADDRESS TO: **Assistant Commissioner for Patents**  
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**Washington, D. C. 20231**

**APPLICATION ELEMENTS**

See MPEP chapter 600 concerning utility patent application contents.

1. X Fee Transmittal Form  
(Submit an original, and a duplicate for fee processing)
2. X Specification (Total Pages 18)  
(preferred arrangement set forth below)
  - Descriptive Title of the Invention
  - Cross References to Related Applications
  - Statement Regarding Fed sponsored R & D
  - Reference to Microfiche Appendix
  - Background of the Invention
  - Brief Summary of the Invention
  - Brief Description of the Drawings (if filed)
  - Detailed Description
  - Claims
  - Abstract of the Disclosure
3. X Drawings(s) (35 USC 113) (Total Sheets 5)
4. X Oath or Declaration (Total Pages 4)
  - a.      Newly Executed (Original or Copy)
  - b.      Copy from a Prior Application (37 CFR 1.63(d))  
(for Continuation/Divisional with Box 17 completed) (**Note Box 5 below**)
  - i.      DELETIONS OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
5.      Incorporation By Reference (useable if Box 4b is checked)  
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. ☐ Microfiche Computer Program (Appendix)

7. ☐ Nucleotide and/or Amino Acid Sequence Submission

(if applicable, all necessary)

- a. ☐ Computer Readable Copy  
b. ☐ Paper Copy (identical to computer copy)  
c. ☐ Statement verifying identity of above copies

**ACCOMPANYING APPLICATION PARTS**

8. ☐ Assignment Papers (cover sheet & documents(s))

9. ☐ a. 37 CFR 3.73(b) Statement (where there is an assignee)

☒ b. Power of Attorney

10. ☐ English Translation Document (if applicable)

11. ☐ a. Information Disclosure Statement (IDS)/PTO-1449

☐ b. Copies of IDS Citations

12. ☐ Preliminary Amendment

13. ☒ Return Receipt Postcard (MPEP 503) (Should be specifically itemized)

14. ☐ a. Small Entity Statement(s)

b. Statement filed in prior application, Status still proper and desired

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APPLICATION FOR UNITED STATES LETTERS PATENT

FOR

METHOD AND APPARATUS TO VERIFY CIRCUIT OPERATING CONDITIONS

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## METHOD AND APPARATUS TO VERIFY CIRCUIT OPERATING CONDITIONS

### BACKGROUND

#### 1. Field

The present invention relates to the field of data verification, and more particularly to verification of the operating conditions of electronic circuits.

#### 2. Background Information

In the modern world, large amounts of information are manipulated and transmitted electronically. Unfortunately, electronic information may be vulnerable to manipulation, tampering, or intrusion by unauthorized third parties. To prevent such unwanted activity, electronic data may be processed in ways which make its contents less vulnerable to intrusion or tampering.

For example, electronic data may be encoded in order to make the contents unrecognizable from its original form. To reduce the risk of unauthorized tampering, the data may be “signed” with a digital signature. Digital signatures may involve the generation and encryption of a unique hash value representing the information, in various manners well known in the art.

Such data operations may be performed using hardware circuits. Use of hardware circuits may increase the speed of such data operations as compared with the use of software executed on a general purpose processor for the same purpose. Hardware circuits may also provide an added security benefit by making it more difficult for unauthorized parties to inspect the logic inherent within the operation.

Unfortunately, unauthorized third parties may attempt to alter the results produced by hardware circuits in an attempt to ascertain the logic within the circuits. One approach

involves the intentional variation of the predetermined operating conditions (voltage, temperature, clock frequency, etc.) of the circuit in order to cause the circuit to output intermediate operation results. For example, a third party may increase the frequency of the clock signal applied to the circuit beyond the maximum predetermined operating frequency of the circuit, which may cause the circuit to output intermediate results of the circuit's operation. Other circuit conditions which may be altered include the operating voltage and operating temperature. An increase in the circuit temperature or a decrease in the operating voltage beyond the circuit's operational limits may cause the circuit to output intermediate results.

Consider a hardware circuit implementing the Digital Encryption Standard:1977 (DES) operation. A complete DES operation may comprise sixteen rounds (iterations) of processing, each subsequent round inputting and operating on the results of the previous round. A synchronous hardware circuit implementing the DES operation may implement multiple rounds (n rounds) of processing per clock cycle. The intermediate result of each n rounds is provided as an input signal for processing during a subsequent clock cycle. After sixteen rounds of processing, the circuit outputs a final result of the DES operation. However, by altering the operating conditions of the circuit it may be possible to cause the circuit to output a final result which represents, for example, only eight rounds of processing. This intermediate result may yield clues about the details of the DES operation which may not be as readily available from the sixteen-round final output of the circuit.

## SUMMARY

A circuit includes an operation unit adapted to perform a circuit operation in a plurality of rounds. The operation unit may operate properly under a predetermined range of operating conditions. The operation unit is adapted to select between receiving an input signal and a test signal and to perform a test round of the circuit operation when the test signal is selected.

The circuit is adapted to compare a reference value with a result of the test round, the reference value identifying a correct value for the result of the test round when the operation unit is operating under the predetermined range of operating conditions. The operation unit is further adapted to receive a disable signal to disable the operation unit from performing the circuit operation when the result of the test round does not match the reference value.

## BRIEF DESCRIPTION OF THE DRAWINGS

The subject matter regarded as the invention is particularly pointed out and distinctly claimed in the concluding portion of the specification. The invention, however, may be further understood by reference to the following detailed description read with reference to the accompanying drawings.

FIG. 1 is a schematic diagram illustrating an embodiment of a circuit to verify circuit operating conditions.

FIG. 2 is a schematic diagram illustrating an embodiment of a circuit to verify cycle-by-cycle circuit clock variations.

FIG. 3 is a timing diagram illustrating the timing of 1) a clock signal to verify, 2) an oscillator output signal, and 3) and AND gate output signal from FIG. 2.

FIG. 4 is a diagram illustrating an embodiment of a method to verify circuit operating conditions.

FIG. 5 is a diagram illustrating an embodiment of a method to verify short-term consistency among clock periods to a circuit.

## DETAILED DESCRIPTION

The embodiments described herein enable an advantageous verification circuit. For example, some embodiments may be implemented to verify both long-term operation conditions of a circuit and cycle-by-cycle variations in clock period. The embodiments described herein are merely illustrative, and one skilled in the art will appreciate that numerous modifications can be made which nonetheless fall within the scope of the present invention.

TABLE 1 shows the intermediate and final results of a DES operation under both normal conditions and conditions in which the operating conditions of the DES circuit have been altered beyond the circuit's normal operating range. The table results assume a two-stage DES unit capable of performing two rounds of DES processing per clock signal.

<b>Clock Signal</b>	<b>Data Input Signal to DES Unit</b>	<b>Output Signal Should Be</b>	<b>Output Signal Is</b>
1	data value	2 round	undefined
2	undefined	4 rounds	2 rounds
3	2 rounds	6 rounds	undefined
4	undefined	8 rounds	4 rounds
5	4 rounds	10 rounds	undefined
6	undefined	12 rounds	6 rounds
7	6 rounds	14 rounds	undefined
8	undefined	16 rounds	8 rounds

TABLE 1

During Clock 1, a data value is applied to the DES unit. Under normal operating conditions, the multistage DES unit performs two rounds of DES processing during a single clock cycle. However, because the operating conditions have been varied (for example, by decreasing the operating voltage, increasing the operating temperature, or

increasing the circuit clock frequency), the DES unit is unable to complete two rounds of DES processing, and the output signal of the DES unit is undefined at the end of the clock period. During Clock 2, the DES unit inputs the output signal produced by the previous round of processing, which is an undefined value. The DES unit performs another two rounds of processing. After the second clock period expires, the output signal of the DES unit is the result of two rounds of processing, because the DES unit has now had sufficient time under the impeded conditions to complete what should have taken a single clock period under normal conditions. During Clock 3, the intermediate result of two rounds of processing is input to the DES unit, and after Clock 4 the output signal of the DES unit reflects four rounds of processing. However, at this time the output signal would have reflected eight rounds of DES processing under normal conditions. After eight clock periods, when the DES operation would normally be complete, the final output signal (the output signal which may be propagated to the output pins of the DES unit) reflects only eight rounds of DES processing; an intermediate result which may yield clues to the value of the DES operation key, for example.

To make it more difficult for third parties to coerce an intermediate result from a DES operation unit, an advantageous circuit may be employed to help detect when the DES unit is operating outside of its predetermined operating range. In one embodiment a DES operation unit inputs two test signals. Processing is performed on these signals and a test output signal is computed. The test output signal may be compared with a stored reference value, the stored reference value being the output signal which the unit should have produced in response to the test signals under normal operating conditions. An indication of equality or inequality between the values may then be produced. An indication of inequality may indicate a variation in the normal operating conditions of the circuit. The circuit may be disabled from further processing upon detection of this situation. Of course, the invention is in no way limited to operation units performing DES; any computational circuit for performing multi-round processing on an input signal may benefit from application of the present invention.



One embodiment of the invention may be useful as a form of tamper protection when, for example, the circuit is to perform a secure operation, such as multiple rounds of DES encoding or decoding. For example, the embodiment may be used to disable the DES circuit from further processing when a third party alters the circuit's operating conditions in an attempt to cause the circuit to output intermediate values of the DES operation.

Referring now to FIG. 1, a schematic diagram illustrating an embodiment 100 of a circuit to verify operating conditions is shown. The embodiment 100 comprises a DES key processor 150 and a DES operation unit 120, although the invention is in no way limited to DES circuits. Those skilled in the art will appreciate that a DES operation may be performed by this circuit by inputting to the key processor 150 a master key signal 175. A variation 140 of the master key signal 175 may be produced by the key processor 150 for each of the sixteen rounds of a DES operation. The DES operation unit 120 may input master key variation signals 140 as well as eight bytes of data to encode 122 during each round of processing. After each round of processing, an intermediate output signal may be produced and stored in register 130 for possible application to the next round of processing. The resulting signal after sixteen rounds of processing is output from the DES operation unit 120 as the final result signal of the DES operation.

In this embodiment multiplexer 110 (a selector circuit) selects as a first input signal to DES unit 120 one of a data signal input 122, a test data signal input 115, and the previous output signal of DES operation unit 120. The output signal produced by key processor 150 is coupled to an input of multiplexer 135. Multiplexer 135 selects between the output signal of key processor 150 and a test key signal 145 as a second input signal to DES operation unit 120. Selecting the output signal of DES operation unit 120 as an input to DES unit 120 provides a feedback loop by which previous intermediate result signals may be provided as input signals to subsequent rounds of DES processing. In this embodiment DES operation unit 120 and key processor 150 may operate synchronously by sharing a common clock signal, and may perform a single round of DES processing per clock cycle. Of course, in an alternate embodiment DES operation unit 120 may

comprise multiple stages of processing and may perform multiple rounds of DES processing per clock cycle.

During a first clock cycle, multiplexer 110 may select the test data signal 115 and multiplexer 135 may select the test key signal 145 as input signals to DES operation unit 120. DES operation unit 120 may operate on these signals and produces a test output signal in register 130, which is compared with reference output value 155 by comparator 160. The reference output value 155 may represent the expected result of a number of rounds of DES processing on the test data signal 122 and test key signal 145. If the values are unequal, an error indication may be produced to disable DES unit 120 from further processing. Otherwise, on a second clock cycle multiplexer 110 may select the data signal 122 and multiplexer 135 may select key signal 140 representing the output signal of key processor 150 as inputs to DES operation unit 120. DES operation unit 120 performs processing on the input data signal 122 and key signal 140 and outputs to register 130 an intermediate result signal representing one round of DES processing. On subsequent clock cycles multiplexer 110 may select the output signal of DES operation unit 120 and multiplexer 135 may select the output signal of key processor 140 as inputs to DES operation unit 120. The output signal of DES operation unit 120 after conclusion of processing may represent the final result signal of the DES operation.

Register 130 coupled to an output port of DES operation unit 120 provides temporary storage for output values of DES unit 120 between clock signals. The output port of register 130 is coupled to multiplexer 110 and comparator 160. When test data signal 115 and test key signal 140 are selected to apply to DES operation unit 120, DES operation unit 120 computes a test output signal which is stored in register 130. Comparator 160 receives test output signal from register 130 upon occurrence of a subsequent clock signal and compares the test output signal with a reference value 155 applied to another input port of comparator. If the test output signal does not match the reference value 155, this may be an indication that the DES operation unit 120 is operating beyond its normal operating conditions. The DES operation unit 120 may be disabled in this circumstance by an indication of inequality signal produced by comparator 160.

As an example of an application of this circuit embodiment, consider what may occur when the frequency of the clock signal applied to DES operation unit 120 is increased beyond the maximum specified operating frequency of the DES unit 120. Referring to TABLE 1, after the first round of processing register 130 may contain an undefined value which may then be received by comparator 160. It is unlikely that this undefined value, not resulting from the signal of a completed computation by DES operation unit 120 on the test signal 122 and test key signal 145, will match reference value 155. Comparator 160 may then produce an indication of inequality which may be used to disable DES operation unit 120 from further processing.

Referring now to FIG. 2, a schematic diagram is provided illustrating another embodiment 200 of a verification circuit, this embodiment to detect cycle-by-cycle clock signal variations. Whereas the embodiment 100 of FIG. 1 may be used to detect longer-term (multiple clock cycle) variations in operating conditions of a circuit, the embodiment 200 of FIG. 2 may be used to detect cycle-by-cycle variations in the clock signal period as applied to a circuit. Cycle-by-cycle clock frequency variations are another technique by which third parties may attempt to cause a circuit to output intermediate results of secure operations. Two units of the circuit embodiment 200 are a clock signal rate sampling unit 202 and an analytical unit 204.

In this embodiment, clock rate sampling unit 202 comprises ring oscillator 225, D flip-flops 210 and 215, AND gate 220, and Johnson counter 230. Numerous modifications and variations to this particular implementation will be apparent to those skilled in the art which nonetheless fall within the scope of the invention. For example, AND gate 220 may be replaced by other logic circuits performing a similar logical function.

Ring oscillator circuits are well known in the art and may be implemented using numerous designs. Although the invention is not limited to the use of ring oscillators, in one embodiment, ring oscillator 225 may be employed comprising an odd number of inverter stages coupled in series, with the output port of the final inverter stage coupled to

the input port of the first inverter stage. In this embodiment the output signal of ring oscillator 225 may comprise the output signal of any of the inverter stages. The output signal of ring oscillator 225 may comprise an alternating sequence of binary 1's and 0's providing a high frequency clocking signal or timebase. In embodiment 200 the output signal of ring oscillator 225 may be supplied as a clock input signal to Johnson counter 230. Johnson counter 230 may increment a count value with each clock signal received from ring oscillator 225.

Johnson counter circuits are well known in the art and may be implemented using numerous designs. Although the invention is not limited to the use of a Johnson counter, in one embodiment a Johnson counter 230 is employed comprising a shift register with the output signal of the final stage inverted and supplied as an input signal to the first stage. The count value output signal of Johnson counter 230 may be provided at output ports at each stage of the shift register, producing a sequence of binary 1's and 0's signals which change by only a single bit with each increment of the count value.

In one embodiment, the output signal of ring oscillator 225 may be supplied as a clock input signal to D flip flops 210 and 215. The D input port of flip flop 210 is coupled to clock signal to verify 205 (not to be confused with the clock output signal produced by ring oscillator 225). D flip flops 210 and 215 may be coupled in such a way that output signal of AND gate 220 is asserted during a period of time during which clock signal 205 transitions from not asserted to asserted state. Output signal of AND gate 220, when asserted, provides a reset signal to Johnson counter 230.

FIG. 3 illustrates the timing of clock signal to verify 205, ring oscillator output signal 225, and AND gate output signal 220. AND gate output signal 220, providing reset signal to counter 230, is asserted for a period of time approximately equal to one period of ring oscillator output signal 225 during the transition of clock signal 205 from a non-asserted level to an asserted level. A result is that reset signal is asserted once during the period of clock signal 205 so that counter 230 counts clock signals from ring oscillator 225 for a full period of clock signal 205.

In one embodiment the frequency of the ring oscillator output signal is much greater than the frequency of clock signal 205 to verify. For example, if the frequency of ring oscillator output signal is 100 times greater than frequency of clock signal 205, counter 230 will produce a count value of approximately 100 between reset signals.

Referring back to FIG. 2, in one embodiment, analytical unit 204 comprises latch 240, Johnson to binary logic 245, sample register 250, reference register 255, subtractor 265 (a circuit to subtract two signals and output a difference signal) and magnitude comparator 270. Latch 240 samples output signal of counter 230 and passes the count signal to logic 245 to convert the Johnson count signal to a binary representation (such as, for example, a one or two's complement number). The converted signal may be stored in sample register 250. If the signal is to serve as a reference value for future comparisons, a reference enable signal 260 may be asserted to enable the count value to be output from sample register 250 to reference register 255. In one embodiment, the reference value may be a count value sampled during a first clock cycle of or immediately preceding an operation by a circuit, such as the DES operation circuit described previously. The signal output by sample register 250 may be subtracted by subtractor 265 from the signal output by reference register 255. The difference may be applied to magnitude comparator 270. Magnitude comparator 270 compares a difference in the values with a limit value 275 and produces an indication 280 when the difference exceeds the limit value. The indication 280 may be an indication that the clock signal 205 is being varied on a cycle-by-cycle basis, and the indication may be used to disable the circuit supplied by clock signal 205.

Referring now to FIG. 4, a diagram illustrating an embodiment 400 of a method to verify circuit operating conditions is shown. During a first clock cycle CLOCK 0, a test data signal is selected at 410 and a test key signal is selected at 420 to apply to a circuit (a DES operation circuit in one embodiment). A number N of rounds of a secure operation, such as a DES operation, is performed at 430, where N is a positive integer. A result of these N rounds of operation is stored at 440.

During a second clock cycle CLOCK 1, which may but is not required to immediately follow first clock cycle CLOCK 0, the test result is compared with a reference value at 450. An indication of the equality of the test value and reference value is output 460. Also during CLOCK 1, a first round of processing may be performed by the circuit by selecting a data value for input 470, selecting a key value for input 480, and processing N rounds of an operation on the data and key values 490. However, if the test result does not compare equally with the reference value, the output indication of inequality may be used to disable the circuit from further processing.

If the test output and reference signals were equal, it may be an indication that the circuit is operating within normal operating conditions. The circuit may then proceed during a third clock cycle CLOCK 2 to process further rounds of the operation, for example in one embodiment by selecting the output signal from the previous N rounds of processing as a next input signal at 415. A key value signal to apply this next input may also be selected at 425. The circuit may then process a next N rounds of the operation at 435.

Referring now to FIG. 5, an embodiment of a method 500 to verify short-term consistency among clock signals to a circuit is shown. During an initial clock cycle CLOCK 0, a count value corresponding to a period of CLOCK 0 is computed at 510 and stored at 520 in a reference register. CLOCK 0 may in some embodiments correspond to CLOCK 0 in FIG. 4 such that computation and storage of the count as in FIG. 5 may occur in parallel with computation of the test value as shown in FIG. 4. During a second clock period CLOCK 1 which may be the next clock period following CLOCK 0, or any clock period during a circuit operation, a count value corresponding to the period of CLOCK 1 is computed at 530. This count value may be subtracted at 540 from the value stored in the reference register during CLOCK 0. The absolute difference may be compared at 550 with a limit value, and if the difference exceeds a limit value, an output indication signal to this effect produced 560.

The output indication may be used to disable the circuit from further processing when the clock period is varied beyond threshold limits during a circuit operation.

In summary, embodiments of an advantageous verification circuit have been disclosed. In one embodiment, operating conditions of a circuit may be verified by comparing the result signal of processing on test input signals with a reference value expected to be produced by the circuit for the test input signals. In another embodiment, cycle-by-cycle variations in clock frequency may be detected by producing a count value for a first clock cycle and comparing with a count value produced for subsequent clock cycles.

While certain features of the invention have been illustrated as described herein, many modifications, substitutions, changes and equivalents will now occur to those skilled in the art. It is, therefore, to be understood that the appended claims are intended to cover all such embodiments and changes as fall within the true spirit of the invention.

What is claimed is:

1. A circuit comprising:

an operation unit adapted to perform a circuit operation in a plurality of rounds, the operation unit to operate properly under a predetermined range of operating conditions, the operation unit adapted to select between receiving an input signal and a test signal and to perform a test round of the circuit operation when the test signal is selected;

the circuit adapted to compare a reference value with a result of the test round, the reference value identifying a correct value for the result of the test round when the operation unit is operating under the predetermined range of operating conditions; and

the operation unit further adapted to receive a disable signal to disable the operation unit from performing the circuit operation, the disable signal produced when the result of the test round does not match the reference value.

2. The circuit of claim 1 in which the circuit operation comprises one of an encryption of decryption operation.

3. The circuit of claim 1 in which the operation unit is further adapted to receive a test key signal and to perform the test round applying the test key signal and the test signal in response to a first clock signal, the circuit adapted to compare the reference value with the result of the test round in response to a subsequent clock signal, the operation unit adapted to select the input signal and perform a first round of the plurality of rounds of the circuit operation applying the input signal in response to the subsequent clock signal.

4. A method comprising:

selecting a test signal to apply to a test round of a circuit operation, the circuit operation comprising a plurality of rounds;



5 comparing a result of the test round with a stored reference value, the stored reference value identifying a correct value for the result of the test round when the circuit is operating under a predetermined range of operating conditions; and producing a disable signal to disable the operation unit from performing the circuit operation when the result of the test round does not match the reference value.

5. The method of claim 4 in which selecting the test signal further comprises:

selecting the test signal and a test key signal to perform one of an encryption or decryption operation by applying the test key signal to the test signal.

6. The method of claim 4 in which in which selecting the test signal further comprises:

selecting the test signal and a test key signal; and

performing the test round applying the test key signal and the test signal in

5 response to a first clock signal.

7. The method of claim 4 in which comparing the result of the test round with a stored reference value further comprises:

selecting an input signal in response to a subsequent clock signal; and

5 comparing the result of the test round with a stored reference value in response to a subsequent clock signal and performing a first round of the plurality of rounds of the circuit operation in response to the subsequent clock signal.

8. A circuit comprising:

a sampling unit to produce a measure of a first frequency of a clock signal applied to the circuit;

5 a memory to store the measure of the first frequency; and

an analytical unit to compare the measure of the first frequency with a measure of a second frequency of the clock signal applied to the circuit, the analytical unit adapted to produce a disable signal to disable the circuit when a difference between the measure of first frequency and the measure of the second

10 frequency exceeds a threshold value.

9. The circuit of claim 8 in which the sampling unit further comprises:

an oscillator adapted to produce a frequency greater than the first and second frequencies of the clock signal; and

5 a counter to count a number of oscillations of the oscillator during a period of the clock signal.

10. The circuit of claim 9 in which the counter comprises a Johnson counter.

11. The circuit of claim 9 in which the analytical unit further comprises:

a subtractor to determine the difference between the measure of first frequency and the measure of the second frequency.

12. The circuit of claim 11 in which the analytical unit further comprises:

a magnitude comparator to receive the difference between the measure of the first frequency and the measure of the second frequency and to produce the disable signal when the difference exceeds a threshold value.

13. A method comprising:

sampling a clock signal applied to a circuit to produce a first frequency sample; storing the first frequency sample;

5 again sampling the clock signal to produce a second frequency sample; comparing the first frequency sample with the second frequency sample; and producing a disable signal to disable the circuit when the difference between the first frequency sample and the second frequency sample exceeds a threshold value.

14. The method of claim 13 further comprising:

producing an oscillation comprising a frequency greater than the frequency of the clock signal; and

5 counting a number of oscillations during a period of the clock signal.

15. The method of claim 13 in which sampling the clock signal further comprises:

producing the first frequency sample during the clock signal when applied to the  
circuit at a start of a circuit operation; and

5 producing the second frequency sample during the clock signal when applied to the  
circuit during the circuit operation.

## ABSTRACT

A circuit includes an operation unit adapted to perform a circuit operation in a plurality of rounds. The operation unit may operate properly under a predetermined range of operating conditions. The operation unit is adapted to select between receiving an input signal and a test signal and to perform a test round of the circuit operation when the test signal is selected.

The circuit is adapted to compare a reference value with a result of the test round, the reference value identifying a correct value for the result of the test round when the operation unit is operating under the predetermined range of operating conditions. The operation unit is further adapted to receive a disable signal to disable the operation unit from performing the circuit operation when the result of the test round does not match the reference value.

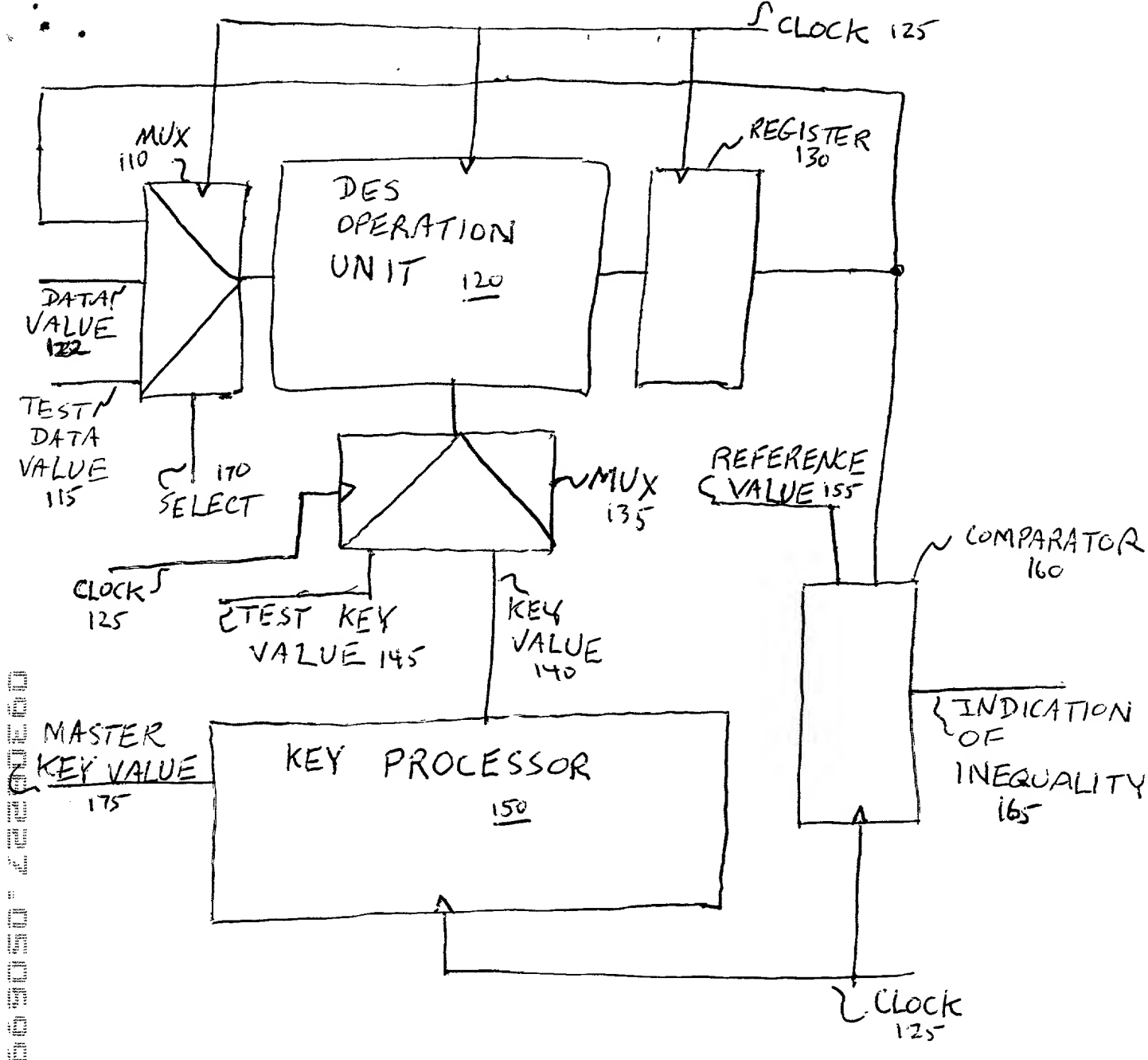


FIG. 1

669090 669090 669090

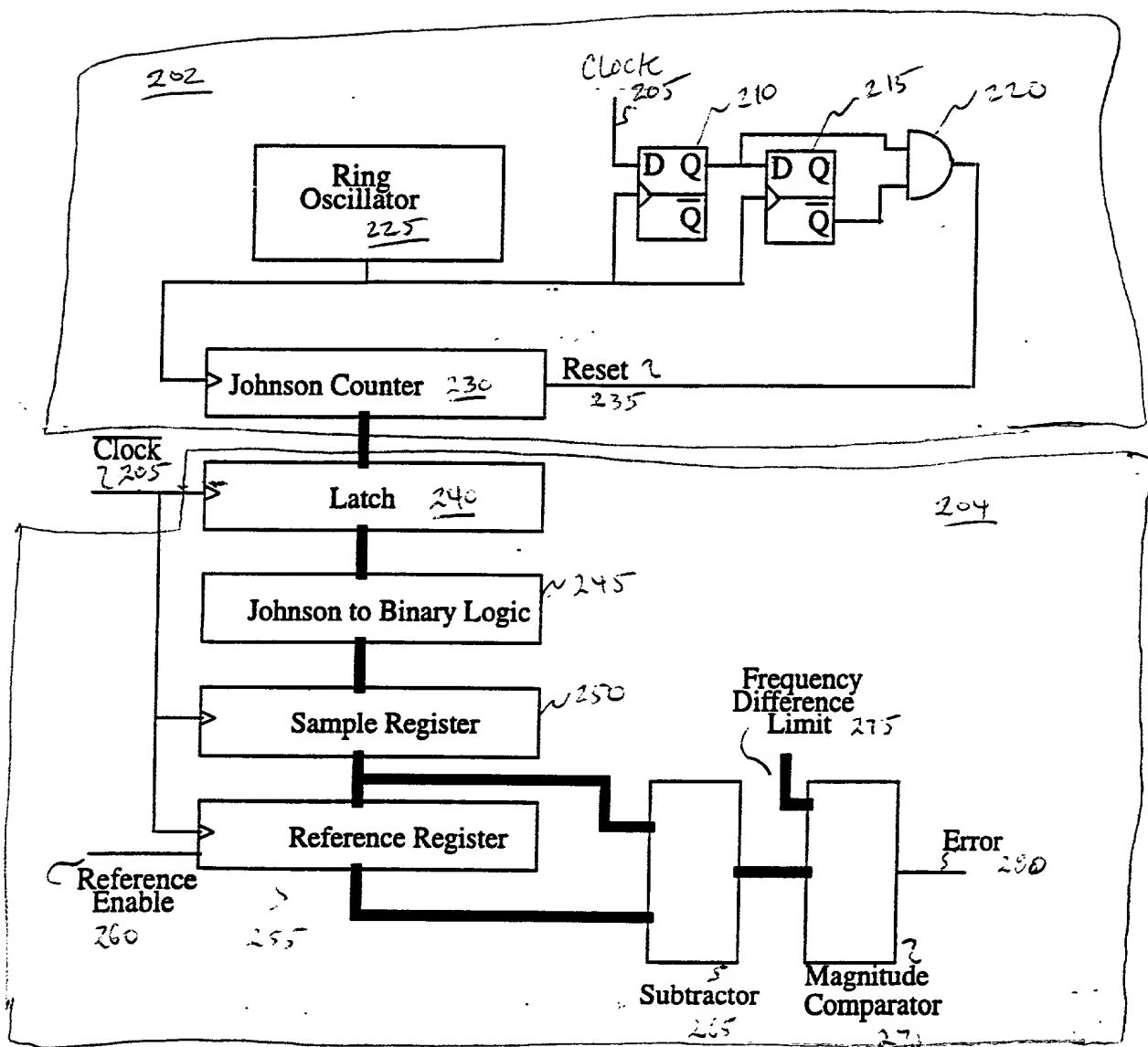


FIG. 1

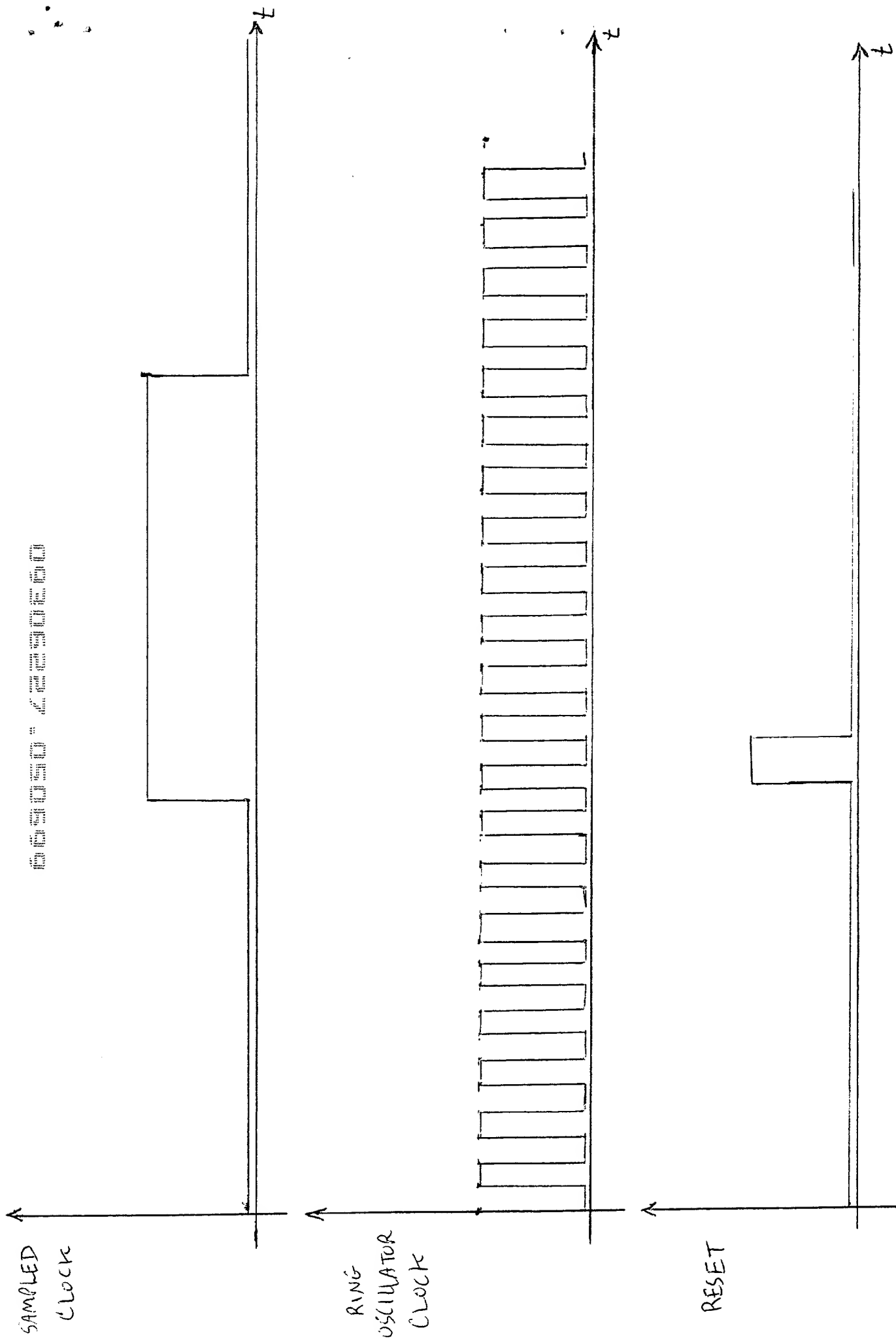


FIG. 3

SELECT TEST DATA VALUE FOR INPUT TO DES UNIT <u>410</u>	SELECT TEST KEY VALUE FOR INPUT TO DES UNIT <u>420</u>	PROCESS N ROUNDS DES OPERATION <u>430</u>	STORE TEST RESULT IN REGISTER <u>440</u>		CLOCK 0
COMPARE TEST RESULT WITH REFERENCE VALUE <u>450</u>	OUTPUT INDICATION OF EQUALITY OF TEST RESULT AND REFERENCE VALUE <u>460</u>	SELECT DATA VALUE FOR INPUT TO DES UNIT <u>470</u>	SELECT KEY VALUE FOR INPUT TO DES UNIT <u>480</u>	PROCESS N ROUNDS DES OPERATION <u>490</u>	CLOCK 1
SELECT OUTPUT OF DES UNIT FOR INPUT TO DES UNIT <u>415</u>	SELECT KEY VALUE FOR INPUT TO DES UNIT <u>425</u>	PROCESS N ROUNDS OF DES OPERATION <u>435</u>			CLOCK 2

FIG. 4

400

669090-22222222



COMPUTE COUNT CORRESPONDING TO CLOCK PERIOD <u>510</u>	STORE COUNT IN REFERENCE REGISTER <u>520</u>			CLOCK 0
COMPUTE COUNT CORRESPONDING TO CLOCK PERIOD <u>530</u>	SUBTRACT COUNT FROM VALUE IN REFERENCE REGISTER <u>540</u>	COMPARE ABSOLUTE DIFFERENCE WITH LIMIT VALUE <u>550</u>	OUTPUT INDICATION OF WHETHER CLOCK PERIOD IS OUTSIDE LIMITS <u>560</u>	CLOCK 1

FIG. 5

500

669350-2220200

Variable	Mean	Standard deviation	Minimum	Maximum
Age	38.5	10.5	25	55
Gender	0.5	0.5	0	1
Marital status	0.7	0.5	0	1
Education	12.5	1.5	10	15
Income	3500	1500	1000	6000
Health	0.8	0.2	0	1
Smoking	0.3	0.5	0	1
Alcohol	0.2	0.4	0	1
Exercise	0.1	0.3	0	1
Stress	0.6	0.4	0	1
Sleep	0.7	0.3	0	1
Work	0.9	0.1	0	1
Family	0.5	0.5	0	1
Friends	0.4	0.4	0	1
Hobbies	0.3	0.3	0	1
Travel	0.2	0.2	0	1
Volunteering	0.1	0.1	0	1
Religion	0.5	0.5	0	1
Politics	0.4	0.4	0	1
Environment	0.3	0.3	0	1
Technology	0.2	0.2	0	1
Art	0.1	0.1	0	1
Music	0.2	0.2	0	1
Gardening	0.1	0.1	0	1
Cooking	0.2	0.2	0	1
Reading	0.3	0.3	0	1
Writing	0.1	0.1	0	1
Photography	0.1	0.1	0	1
Fishing	0.1	0.1	0	1
Hiking	0.1	0.1	0	1
Swimming	0.1	0.1	0	1
Yoga	0.1	0.1	0	1
Meditation	0.1	0.1	0	1
Journaling	0.1	0.1	0	1
Volunteering	0.1	0.1	0	1
Religion	0.5	0.5	0	1
Politics	0.4	0.4	0	1
Environment	0.3	0.3	0	1
Technology	0.2	0.2	0	1
Art	0.1	0.1	0	1
Music	0.2	0.2	0	1
Gardening	0.1	0.1	0	1
Cooking	0.2	0.2	0	1
Reading	0.3	0.3	0	1
Writing	0.1	0.1	0	1
Photography	0.1	0.1	0	1
Fishing	0.1	0.1	0	1
Hiking	0.1	0.1	0	1
Swimming	0.1	0.1	0	1
Yoga	0.1	0.1	0	1
Meditation	0.1	0.1	0	1
Journaling	0.1	0.1	0	1

PATENT

**DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION**  
**(FOR INTEL CORPORATION PATENT APPLICATIONS)**

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

## METHOD AND APPARATUS TO VERIFY CIRCUIT OPERATING CONDITIONS

the specification of which

X is attached hereto.  
\_\_\_\_\_ was filed on \_\_\_\_\_ as  
United States Application Number \_\_\_\_\_  
or PCT International Application Number \_\_\_\_\_  
and was amended on \_\_\_\_\_  
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

<u>Prior Foreign Application(s)</u>			<u>Priority Claimed</u>	
_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	Yes	No
_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	Yes	No
_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	Yes	No

I hereby claim the benefit under title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below

_____ (Application Number)	_____ Filing Date
_____ (Application Number)	_____ Filing Date

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

_____ (Application Number)	_____ Filing Date	_____ (Status -- patented, pending, abandoned)
_____ (Application Number)	_____ Filing Date	_____ (Status -- patented, pending, abandoned)

I hereby appoint Farzad E. Amini, Reg. No. P42,261; Aloysius T. C. AuYeung, Reg. No. 35,432; Amy M. Armstrong, Reg. No. 42,265; William Thomas Babbitt, Reg. No. 39,591; Carol F. Barry, Reg. No. 41,600; Jordan Michael Becker, Reg. No. 39,602; Bradley J. Berezna, Reg. No. 33,474; Michael A. Bernadieu, Reg. No. 35,934; Roger W. Blakely, Jr., Reg. No. 25,831; Gregory D. Caldwell, Reg. No. 39,926; Kent M. Chen, Reg. No. 39,630; Lawrence M. Cho, Reg. No. 39,942; Yong S. Choi, Reg. No. P43,324; Thomas M. Coester, Reg. No. 39,637; Roland B. Cortes, Reg. No. 39,152; Barbara Bokanov Courtney, Reg. No. 42,442; Michael Anthony DeSanctis, Reg. No. 39,957; Daniel M. De Vos, Reg. No. 37,813; Robert Andrew Diehl, Reg. No. 40,992; Tarek N. Fahmi, Reg. No. 41,402; James Y. Go, Reg. No. 40,621; Richard Leon Gregory, Jr., Reg. No. 42,607; Dinu Gruia, Reg. No. P42,996; David R. Halvorson, Reg. No. 33,395; Thomas A. Hassing, Reg. No. 36,159; Phuong-Quan Hoang, Reg. No. 41,839; Willmore F. Holbrow III, Reg. No. P41,845; George W. Hoover II, Reg. No. 32,992; Eric S. Hyman, Reg. No. 30,139; Dag H. Johansen, Reg. No. 36,172; William W. Kidd, Reg. No. 31,772; Michael J. Mallie, Reg. No. 36,591; Andre L. Marais, under 37 C.F.R. § 10.9(b); Paul A. Mendonsa, Reg. No. 42,879; Darren J. Milliken, Reg. No. 42,004; Thinh V. Nguyen, Reg. No. 42,034; Kimberley G. Nobles, Reg. No. 38,255; Michael A. Proksch, Reg. No. 43,021; Babak Redjaian, Reg. No. 42,096; James H. Salter, Reg. No. 35,668; William W. Schaal, Reg. No. 39,018; James C. Scheller, Reg. No. 31,195; Anand Sethuraman, Reg. No. P43,351; Charles E. Shemwell, Reg. No. 40,171; Maria McCormack Sobrino, Reg. No. 31,639; Stanley W. Sokoloff, Reg. No. 25,128; Judith A. Szepesi, Reg. No. 39,393; Vincent P. Tassinari, Reg. No. 42,179; Edwin H. Taylor, Reg. No. 25,129; George G. C. Tseng, Reg. No. 41,355; Lester J. Vincent, Reg. No. 31,460; John Patrick Ward, Reg. No. 40,216; Stephen Warhola, Reg. No. 43,237; Charles T. J. Weigell, Reg. No. 43,398; Ben J. Yorks, Reg. No. 33,609; and Norman Zafman, Reg. No. 26,250; my attorneys, and James A. Henry, Reg. No. 41,064; Daniel E. Ovanezian, Reg. No. 41,236; Glenn E. Von Tersch, Reg. No. 41,364; and Chad R. Walsh, Reg. No. 43,235; my patent agents, of BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP, with offices located at 12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025, telephone (310) 207-3800, and Alan K. Aldous, Reg. No. 31,905; Robert D. Anderson, Reg. No. 33,826; Joseph R. Bond, Reg. No. 36,458; Richard C. Calderwood, Reg. No. 35,468; Cynthia Thomas Faatz, Reg. No. 39,973; Sean Fitzgerald, Reg. No. 32,027; Seth Z. Kalson, Reg. No. 40,670; David J. Kaplan, Reg. No. 41,105; Leo V. Novakoski, Reg. No. 37,198; Naomi Obinata, Reg. No. 39,320; Thomas C. Reynolds, Reg. No. 32,488; Steven P. Skabrat, Reg. No. 36,279; Howard A. Skaist, Reg. No. 36,008; Steven C. Stewart, Reg. No. 33,555; Raymond J. Werner, Reg. No. 34,752; and Charles K. Young, Reg. No. 39,435; my patent attorneys, and Jeffrey S. Draeger, Reg. No. 41,000; Thomas Raleigh Lane, Reg. No. 42,781; Calvin E. Wells, Reg. No. P43,256; and Alexander Ulysses Witkowski, Reg. No. P43,280; my patent agents, of INTEL CORPORATION; and James R. Thein, Reg. No. 31,710, my patent attorney; with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

Send correspondence to Charles A. Mirho, Intel Corporation, c/o BLAKELY, SOKOLOFF,  
(Name of Attorney or Agent)

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(Name of Attorney or Agent)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Sole/First Inventor Roy Callum

Inventor's Signature \_\_\_\_\_ Date \_\_\_\_\_

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